Secure Gateway-V1.1

For AURIX™ family

About this document

Scope and purpose

This document describes the features and hardware details of the Secure Gateway-V1.0 and V1.1 equipped with an TriCore AURIX™ Microcontroller from Infineon Technologies AG.

Intended audience

This document is intended for anyone who wants to develop software on the Secure Gateway-V1.0 and V1.1 or wants to use this kit for evaluating and demonstrating the capabilities of the AURIX™ microcontroller in combination with other Infineon Technologies products.

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1 Introduction of the Secure Gateway V1.1

The Secure Gateway-V1.1 offers a huge range of Application use cases. With the AURIX™ TC377TX in combination with Marvell's 88Q5050 Switch and 88Q2112 1000Base-T1 PHY future In Vehicle Networks can be addressed and evaluated. The TC377TX featured with two Gigabit Ethernet Ports is connected with a 1Gbps RGMII port to the Ethernet Switch for data transfer. The second Ethernet port of the TC377TX is connected to a 1000Base-T PHY from Marvell. The 88Q5050 provide five 100Base-T1 Ports together with the Rosenberger H-MTD® connector. Two 1000Base-T1 PHYs from Marvell in addition provide the right feature set to connect the Secure Gateway-V1.1to an In Vehicle Network. 12 CAN-FD connections with various kinds of Infineon's CAN transceiver, 2 LIN and 2 FlexRay channels allow bridging of different network topologies. And extension header allow to connect additional components to the board via a 1Gb SGMII Ethernet connection. The TC377TX provides the HSSL interface, a QSPI and I2C channel on this connector.

AURIX™ TC3xx does not compromise on security. The second generation of the programmable Hardware Security Module (HSM) is available across the family for secure on-board communications and to prevent hardware manipulation such as tuning. Infineon's Trusted Platform Module (TPM) SLB9670 is the latest product featuring a fully TCG TPM 2.0 standard compliant module connected via SPI to the AURIX™.

1.1 Key features

- AURIX™ TC377TX with two Gigabit Ethernet Ports
- Infineon Supply IC's TLF30682QVS01, TLS4125V50, TLS203B0, IR3883
- Infineon CAN transceivers TLE9250, TLE9252, TLE9254, TLE9255 (partial Network capabilities)
- Infineon LIN transceiver TLE7258 and Flexray transceiver TLE9222
- Infineon TPM SLB9670VQ2.0
- Marvell 88Q5050 Switch and 88Q2112 and 88EA1512 Ethernet PHYs

1.2 Block diagram

The block diagram in Figure 1 shows the main components of the Secure Gateway-V1.1 and interconnects between the used devices.

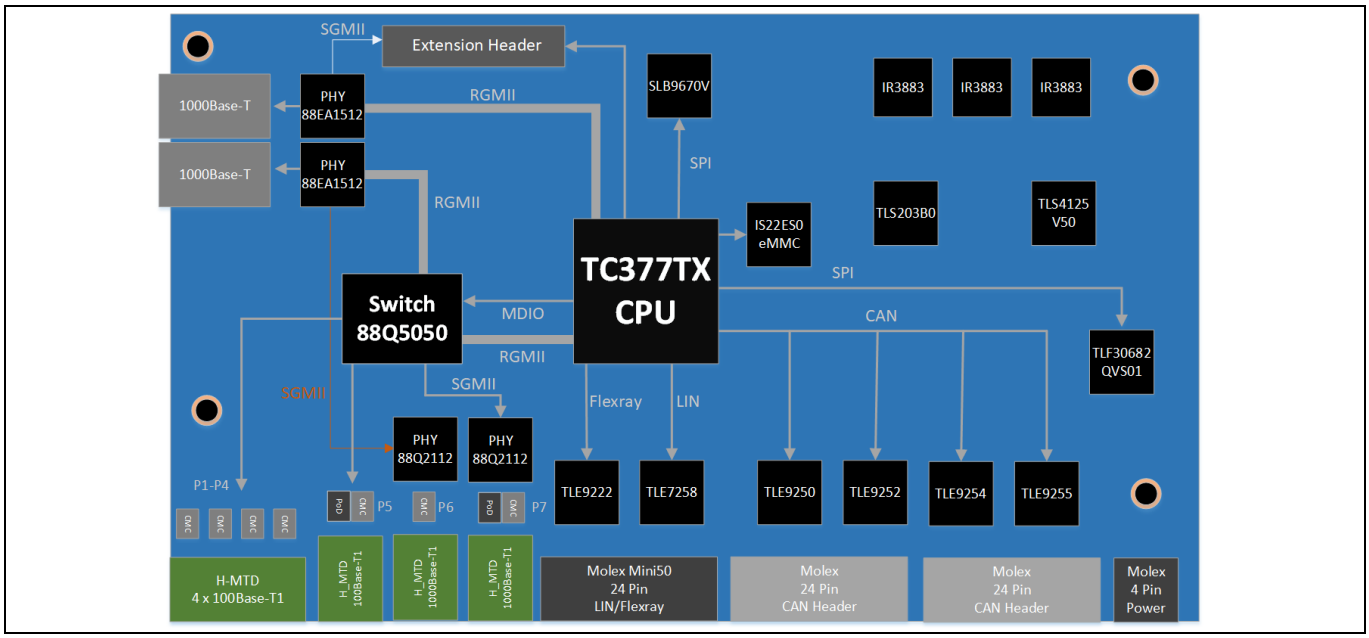

Figure 1 Block diagram of the Gateway Board

2 Hardware description

The following chapters provide a detailed description of the hardware and how it can be used.

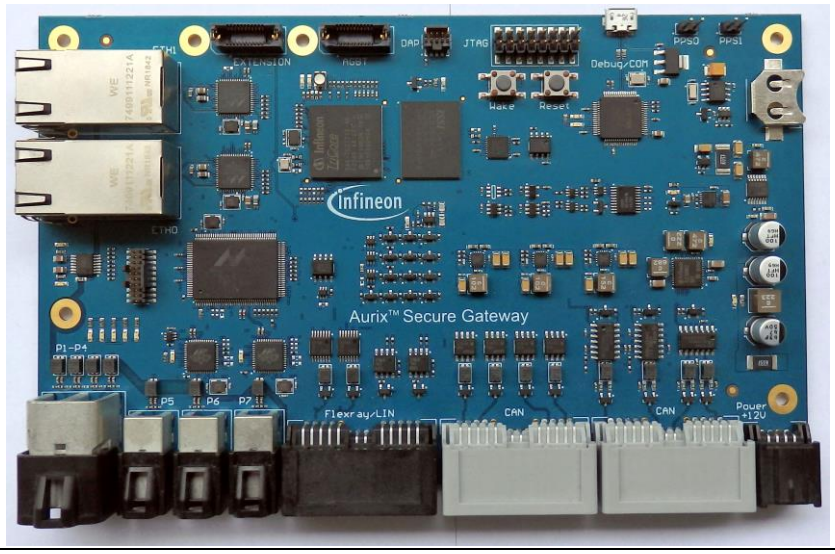

Figure 2 PCB of the Secure Gateway-V1.1

2.1 Power supply

The Power Supply concept must guarantee a stable supply of the Board. The standard Input voltage is 12V. Out of several voltages will be generated. Figure 3 visualize the power domains and used structure of Infineon's supply IC behind.

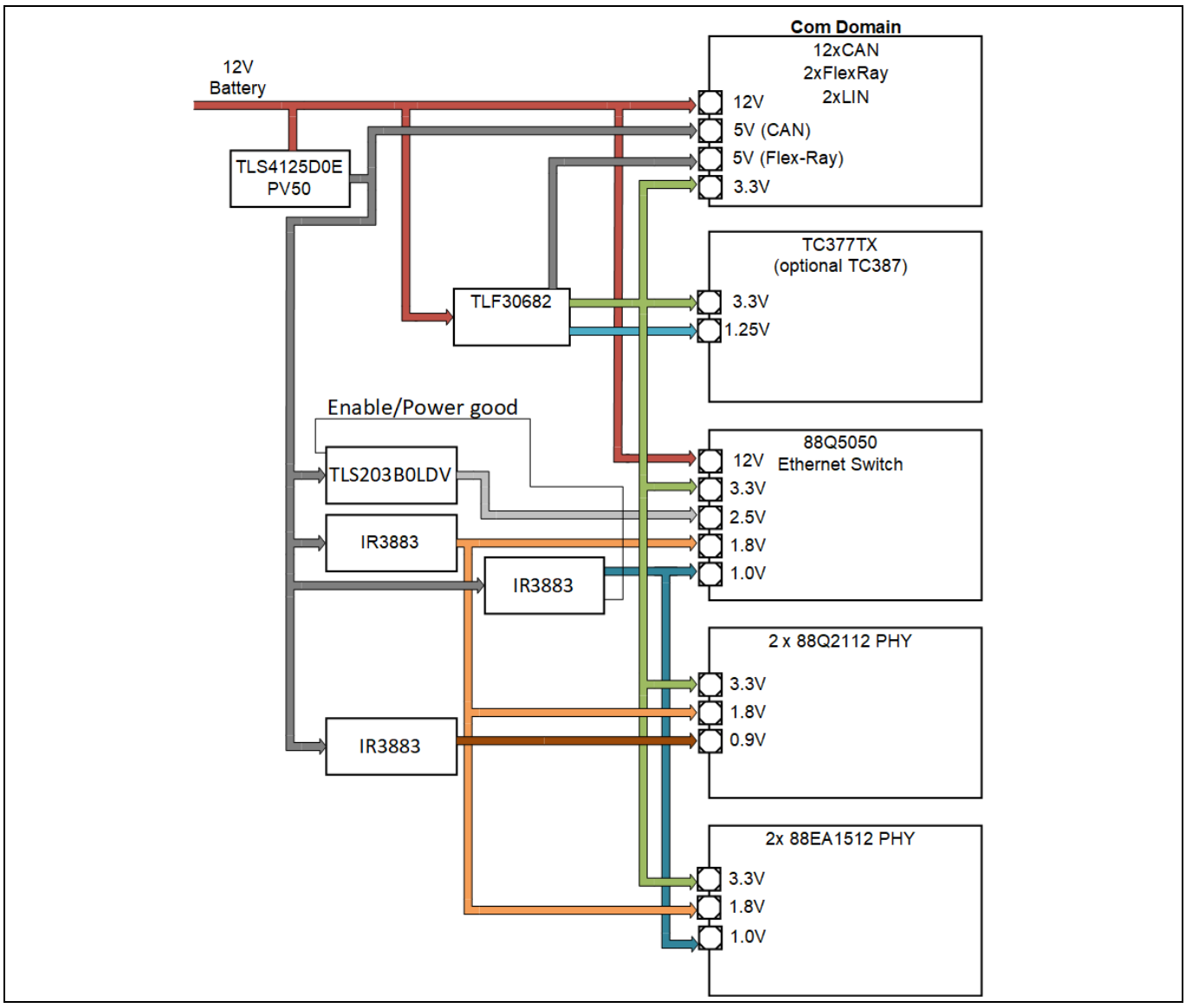

Figure 3 Supply structure

2.1.1 TLF30682QVS01

The TLF30682QVS01, member of the OPTIREG™ PMIC-family, is a multi-rail supply for ADAS-applications like 76-79 GHz-Radar, multi-purpose Camera, or Display, Cluster, or Center Stack applications.

It's using an efficient and flexible pre-/post-regulator concept over a wide input voltage range. The high switching frequency range of the battery connected, synchronous buck (3V3/3.5A) with integrated switches allows optimization in usage of small filter components. An integrated synchronous SMPR-buck (Switch-Mode Post-Regulator) with high switching frequency enables supply for core or for memory (0V9-1V3/2.0A). Additionally, an asynchronous SMPR-boost (5V0/0.25A), running as well with high switching frequency,

provides the 5V-domain for transceiver. Integrated switches, compensation and the high switching frequency is both minimizing the number and the value of external components required.

Additional features are under-/over-voltage monitoring (via independent reference) of all integrated and up to two external rails as well as a flexible watchdog concept to supervise the µC offers high flexibility for multiple applications.

The automotive qualified TLF30682QVS01 is coming in small, thermally enhanced VQFN-48 capable for automated optical inspection.

The TLF30682QVS01 is PRO-SIL™ ISO26262-Ready, functional safety documents are available on request (for more info visit **www.infineon.com/PRO-SIL**).

The device provides the following features:

- Step-down pre-regulator for wide input voltage range from 3.7 to 35 V (40 V limited time) with low overall power loss and fast transient performance. Suitable for operation with ceramic capacitors
- High-efficiency step-down post regulator for second output voltage generation
- Step-up post regulator with 5 V output voltage
- Voltage monitoring for two external voltage rails including enable signals
- 16-bit SPI interface to host CPU
- Configurable window watchdog

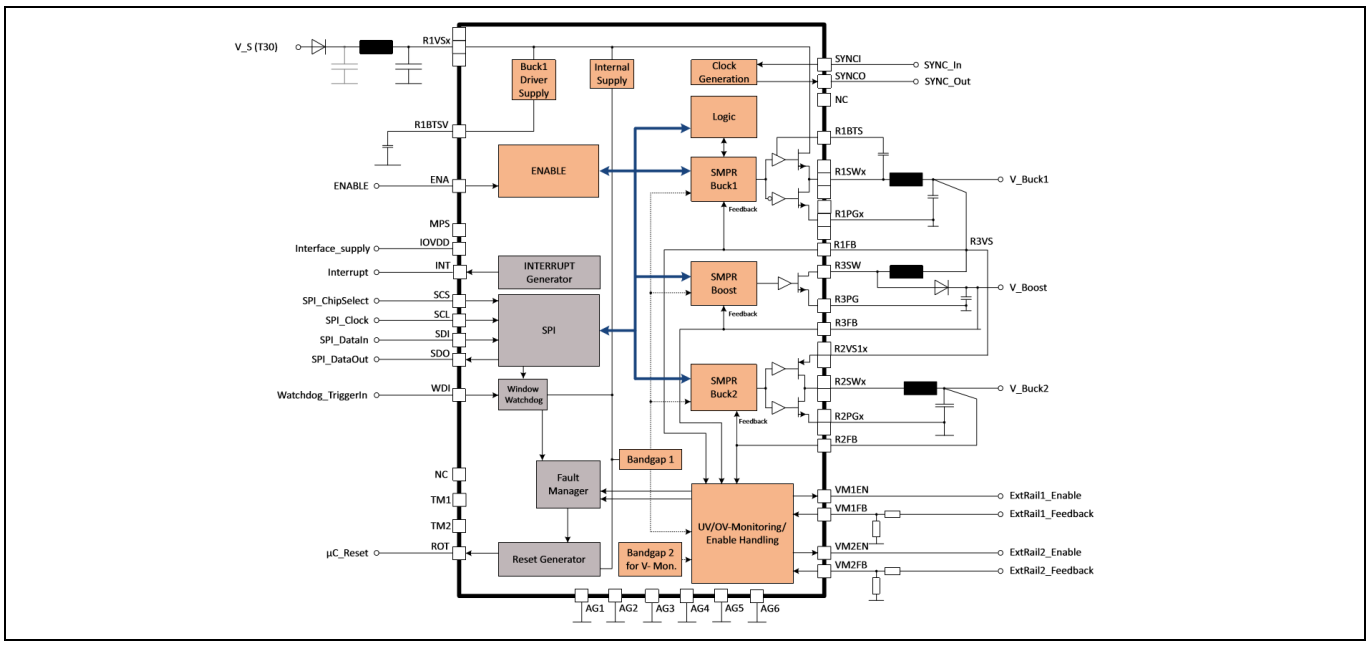

Figure 4 TLF30682QVS01 Block Diagram

Table 1 shows the signal connection list for the connection between CPU A and the TLF30682QV01.

Table 1 Connection between CPU A and TLF30682QVS01

CPU	Module	Signal	Pin	Comment
CPU	QSPI4	SLSO3	P22.2	SLSO3
CPU	QSPI4	SCLK	P22.3	
CPU	QSPI4	MTSR	P22.0	

CPU	QSPI4	MRST	P22.1	
CPU	ESR	INT	/ESR1	
CPU	Reset	/PORST	/PORST	
CPU	I/O	WDI	P40.6	

2.1.2 Power supply sequencing and power down

The Secure Gateway-V1.1supply is converted into several different voltage domains. Powering up the board will switch on the cascaded voltage ICs.

There is a global 12V INH signal named V_ENA_12V which can switch off all DC/DC on the Board. This signal is generated out of a logic AND from the INH signals coming from Marvell's 88Q5050 Switch and the two 1000Base-T1 PHYs 88Q2112.

The Automotive Ethernet network sleep and wake-up concept is designed to save maximum power of car ECUs. Open Alliance working group TC10 describes the concept used in 100/1000Base-T1.

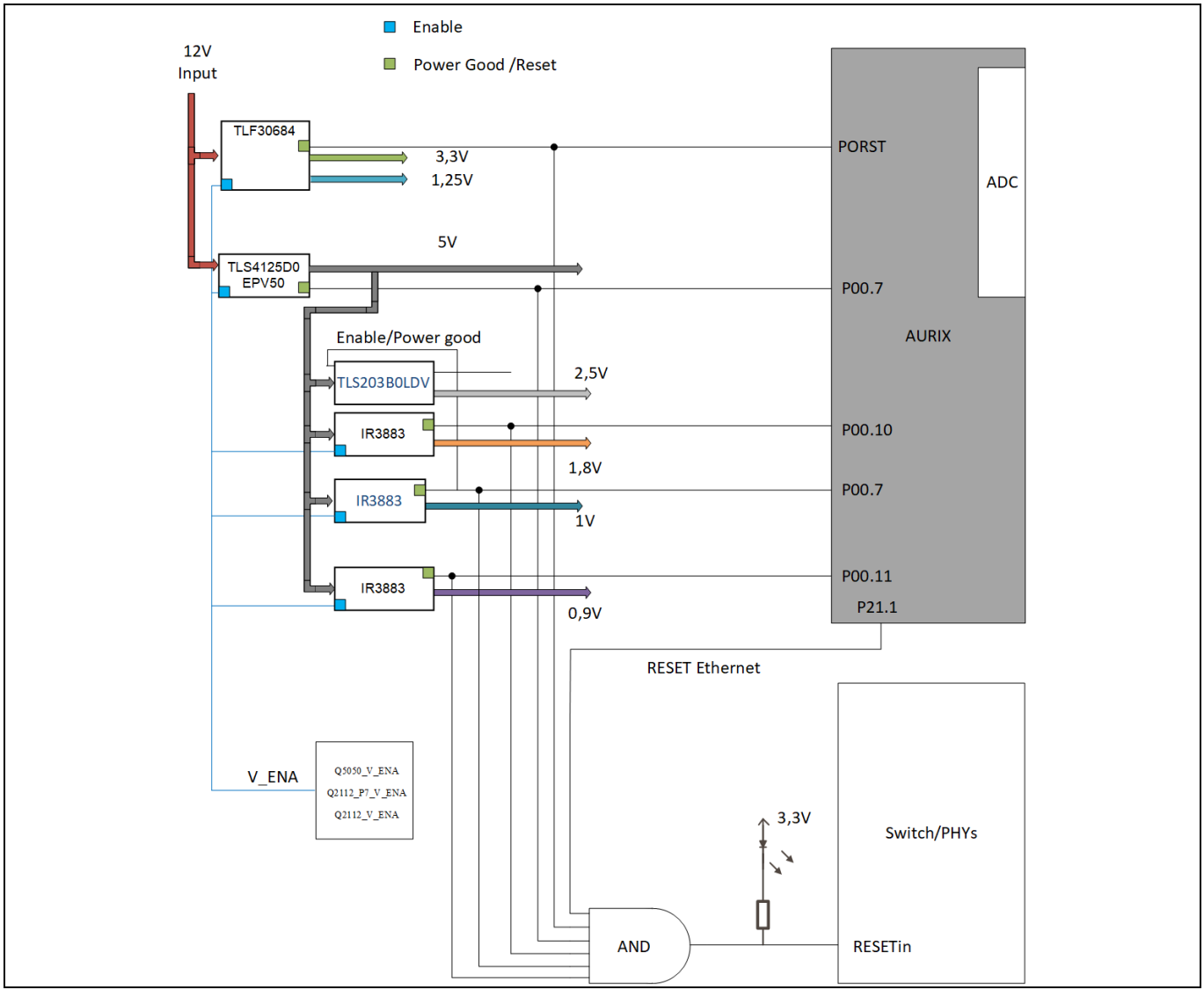

Figure 5 Board power validation

2.1.3 Supply Monitoring functions

The Secure Gateway-V1.1provide several monitoring functions to determine the correct voltage levels, acting according violations and provide these as meta data to higher management functions.

The following tables list the signals connected to the VADC of TC377TX.

Table 2 Analog Signals to TC377TX

Module	Signal	ADC Kernel	Comment
VADC	AN0		+12V analog signal
VADC	AN1		+5V analog signal
VADC	AN2		+3,3 analog signal
VADC	AN3		+2,5V analog signal
VADC	AN4		+1,8V analog signal
VADC	AN5		+1,25V analog signal
VADC	AN6		+1V analog signal
VADC	AN7		+0,9 analog signal
VADC	AN8		+12V Board input rail current
VADC	AN9		+5V rail current generated by TLS4125D0EPV50
VADC	AN10		BTS7008-2EPA feedback

2.2 Gateway Board Resets

The Secure Gateway-V1.1features several reset sources and groups depending on connected devices. The TC377TX reset source is the /PORST signal driven by the TLF30682QV01.

The reset of Marvell's Ethernet components is generated out of power good signals coming from the DC/DC converters and the TC377TX Pin P21.1. By default this signal shell be pulled high so that the Marvel components booting up. The red LED D201 signalizes the active reset state if the LED is on. The device U901 88Q2112 in addition is be forced into reset by pin P32.3 of the TC377TX which is pulled low by an external resistor.

The SLB9670VQ2.0 per default can be reset by P14.8 from TC377TX. Optionally he can be reset by TC377TX /ESR0 signal upon adapting the zero ohm bridges.

The eMMC per default gets reset by P00.6. Optionally he can be reset by TC377TX /ESR0 signal upon a software reset adapting the zero ohm bridges.

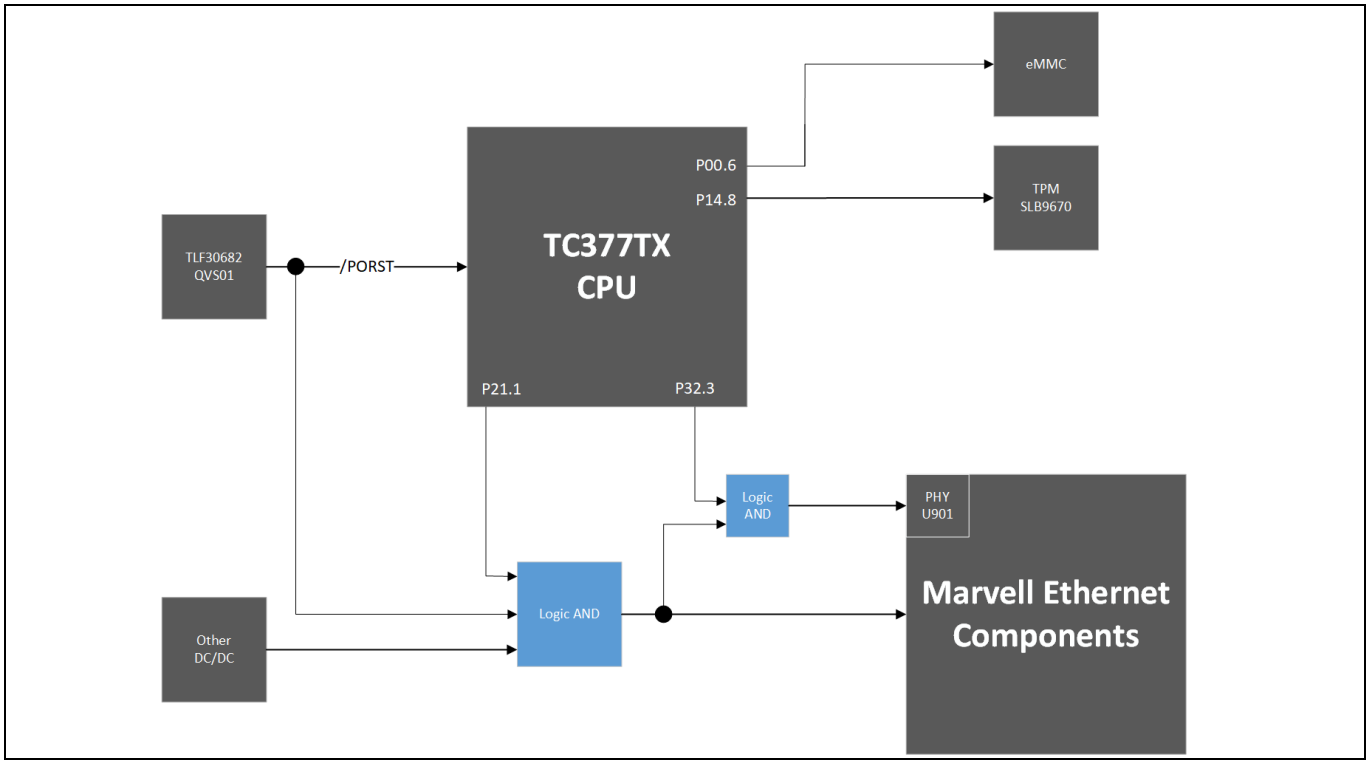

Figure 6 Reset connections

2.3 AURIX™ 2G CPU to Switch connections

The AURIX™ TC377TX provides two 1Gbit Ethernet MAC's using RGMII to connect a Switch or PHY. On the Secure Gateway-V1.1the AURIX™ device is connected via GMAC0 RGMII interface to Marvell's 88Q5050 switch on Port 8. As Switch Management interface the MDIO channel is connected. As well 88Q5050 switch port 8 is acting as RMU port to manage the switch.

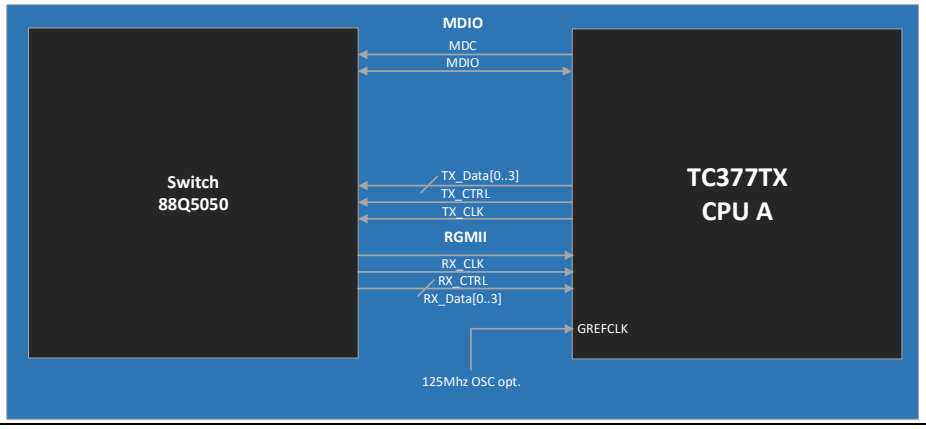

Figure 7 AURIX™ 2G CPU to 88Q5050 Switch connections

Beside the standard RGMII signals the AURIX™ needs a 125MHz reference clock called GREFCLK for the Gb Ethernet Interface. By default this clock will be generated a crystal oscillator. In addition there is the option on the Secure Gateway-V1.1to use a reference clock from a PHY for GREFCLK selectable via a resistor jumper.

Attention: If the 125MHz GREFCLK is not present, the GMAC will not execute the DMA_MODE.SWR software reset.

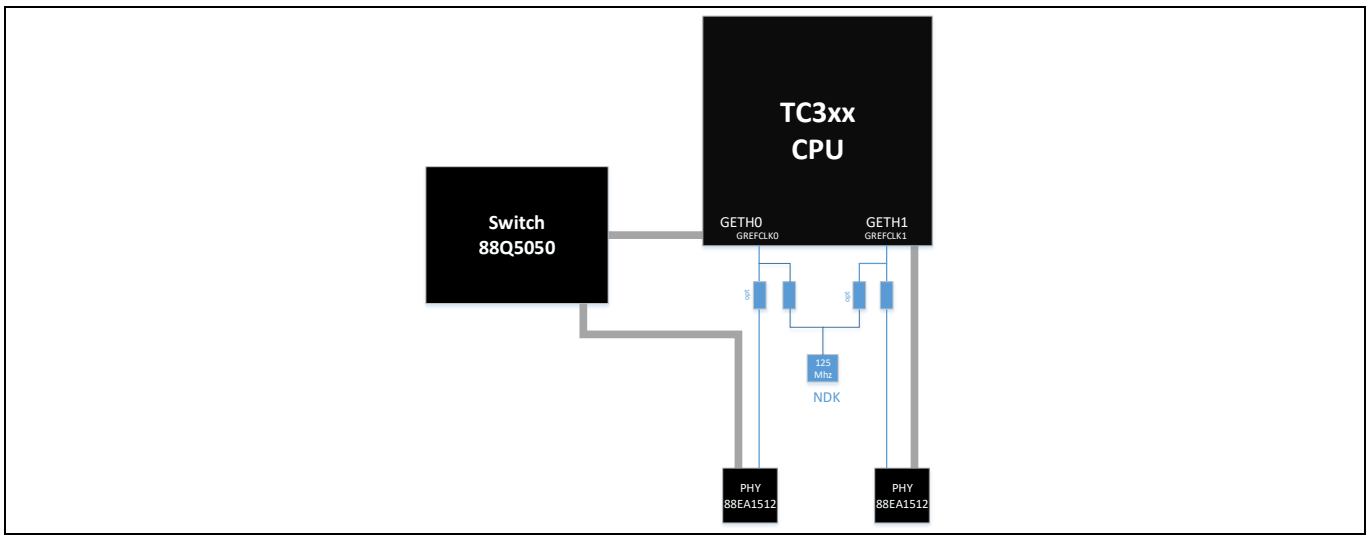

Figure 8 GMAC GREFCLK selection scheme

Table 3 shows the signal connection list for the connection between CPU and the Ethernet Switch.

Table 3 Connection between TC377TX and the Ethernet Switch

Module	Signal	Pin	Comment
GMAC	TXD0_0	P11.3	GETH_TXD0
GMAC	TXD1_0	P11.2	GETH_TXD1
GMAC	TXD2_0	P11.1	GETH_TXD2
GMAC	TXD3_0	P11.0	GETH_TXD3
GMAC	TCTL_0	P11.6	GETH_TCTL
GMAC	TXCLK_0	P11.4	GETH_TXCLK
GMAC	RXD0_0	P11.10	GETH_RXD0
GMAC	RXD1_0	P11.9	GETH_RXD1
GMAC	RXD2_0	P11.8	GETH_RXD2
GMAC	RXD3_0	P11.7	GETH_RXD3
GMAC	RCTL_0	P11.11	GETH_ RXCTLA
GMAC	RXCLK_0	P11.12	GETH_RXCLKA
GMAC	REFCLK_0	P11.5	GETH_GREFCLK

2.4 AURIX™ 2G CPU to PHY connections

The AURIX™ TC377TX offers a second instance of the Ethernet MAC (GMAC), GMAC1. The Interface is connected via RGMII to an 88EA1512 PHY of Marvell. The GMAC1 as well needs a 125MHz reference clock with same requirements of GMAC0. Please refer to Figure 8.

Table 4 show the signals between the GMAC1 and the 88EA1512 PHY.

Table 4 Connection between TC377TX and the Ethernet PHY

Module	Signals	Pin	Comment
GMAC	TXD0_1	P22.10	GETH1_TXD0
GMAC	TXD1_1	P23.4	GETH1_TXD1
GMAC	TXD2_1	P23.3	GETH1_TXD2
GMAC	TXD3_1	P23.2	GETH1_TXD3
GMAC	TCTL_1	P22.11	GETH1_TXCTL
GMAC	TXCLK_1	P22.12	GETH1_TXCLK
GMAC	RXD0_1	P22.4	GETH1_RXD0
GMAC	RXD1_1	P23.7	GETH1_RXD1
GMAC	RXD2_1	P23.6	GETH1_RXD2
GMAC	RXD3_1	P23.5	GETH1_RXD3
GMAC	RCTL_1	P22.6	GETH1_ RXCTLA
GMAC	RXCLK_1	P22.5	GETH1_RXCLKA
GMAC	REFCLK_1	P22.7	GETH1_GREFCLK

2.5 AURIX™ Ethernet MAC Address EEPROM

The Secure Gateway-V1.1supports an I2C EEPROM and a Real-Time-Clock (RTC) with two a unique MAC address. Software can load these and use it to configure the Ethernet GMAC's.

Table 5 Ethernet MAC Address EEPROM

Module	Signal	Pin	Comment
I2C	SCL	P13.1	
I2C	SDA	P13.2	

2.6 MDI Address configuration

The Ethernet devices on the Secure Gateway-V1.1are connected via the MDIO Bus together and can be addressed by the given address list in Table 6.

Table 6 MDI address list

Device	Module	Address	Comment
88Q5050 Slave	GETH 0	0x01	
88Q2112 (U900)	GETH 0	0x02	
88Q2112 (U901)	GETH 0	0x03	
88EA1512 (U1000)	GETH 0	0x04	
88EA1512 (U1001)	GETH 1	0x01	

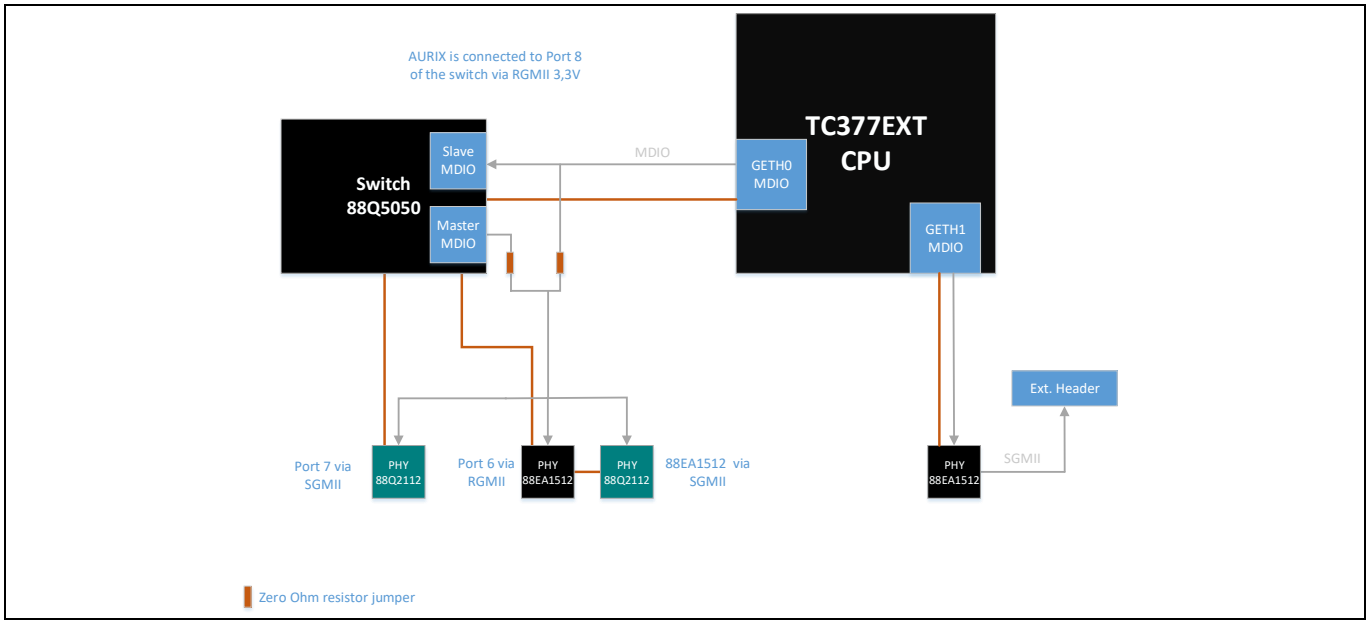

Figure 9 MDI Bus structure

2.7 TC377TX Ethernet PPS signal

Both Ethernet MAC provide a PPS signal which can be selected on a GPIO. For GMAC the GPIO pin used is P14.4. For GMAC1 the GPIO pin used is P21.0. Both signals are available on a pin header.

2.8 Marvell Ethernet Components

To find out more about Marvell's Switch and PHY please contact the listed contact partner in Appendix A.

2.8.1 1000/100Base-T1 CMC and PoDL

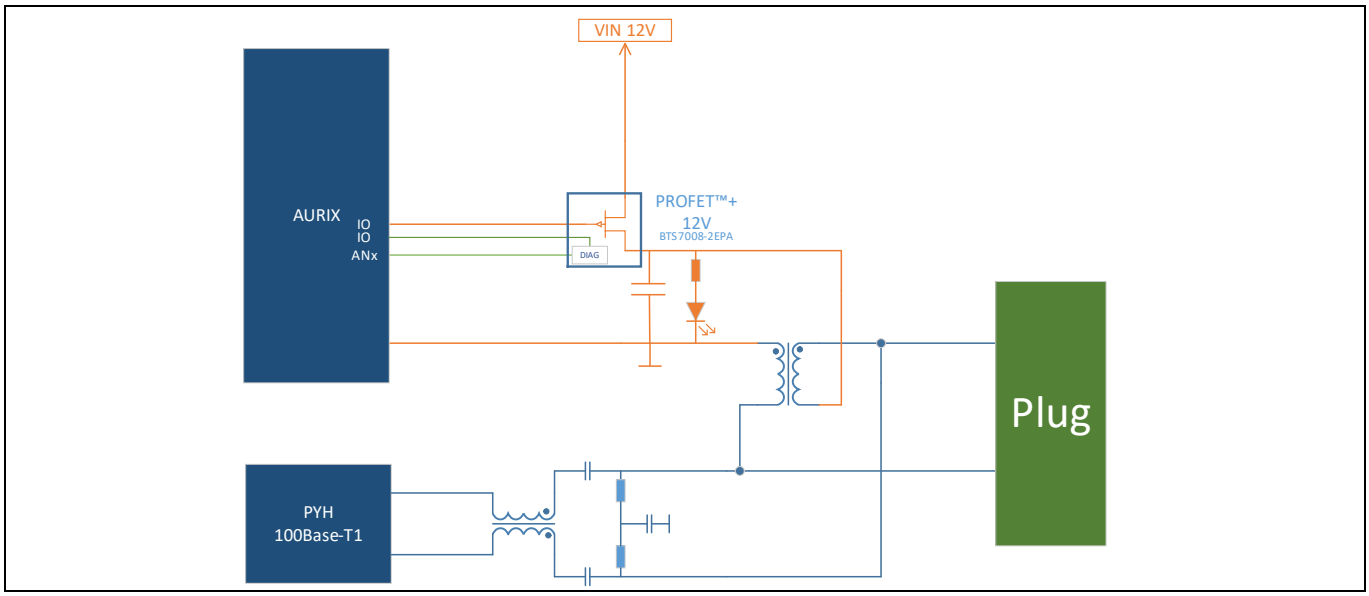

Figure 10 CMC and PODL schematic

Table 7 shows the PoDL signal connection list.

Table 7 PoDL Signal List

Module	Signal	Pin	Comment
I/O	IN0	P32.4	Port ETH_P5 power enable
I/O	IN1	P01.5	Port ETH_P7 power enable
I/O	DEN	P32.5	Port ETH_P5 and ETH_P7 diagnose enable
I/O	DSEL	P01.6	Port ETH_P5 and ETH_P7 channel select
AN	IS	AN10	Diagnose feedback ETH_P5 and ETH_P7

2.8.2 Standard 1000Base-T1 / 100Base-T1 connector

Rosenberger H-MTD® is a 360° fully shielded differential connector system. The new developed system combines high-performance data transmission up to 15 GHz or 20 Gbps and a small package size in a robust automotive grade housing. H-MTD® Cable and PCB connectors are available as single, double, quad for STP, UTP and SPP cables.

Figure 11 Rosenberger H-MTD

2.8.3 Standard 1000Base-T1 / 100Base-T1 quad-connector

Rosenberger H-MTD® is a 360° fully shielded differential connector system. The new developed system combines high-performance data transmission up to 15 GHz or 20 Gbps and a small package size in a robust automotive grade housing. H-MTD® Cable and PCB connectors are available as single, double, quad for STP, UTP and SPP cables.

Figure 12 Rosenberger H-MTD

To find out more about Rosenberger H-MTD® please contact the listed contact partner in Appendix A. Figure 13 show the Marvell switch port coding of the quad Rosenberger H-MTD® connector.

Figure 13 4 Port Rosenberger H-MTD to Marvell coding

2.8.4 1000Base-TX Magnetics and RJ45 Jack

To connect the Secure Gateway-V1.1to a standard IT infrastructure two RJ45 jacks for voltage driven PHYs provide CAT6/CAT7 cables connections. One Gbit Ethernet port is connected as port 6 to the 88Q5050 Switch, the second is connected to AURIX GMAC1 over the 88EA1512 Marvell PHY.

Figure 14 Magnetics and RJ45 Jack

2.9 Molex Mini50 CAN-FD

There are two Molex Mini50 connectors (X1110, X1107) for CAN-FD connections on the Secure Gateway-V1.1In sum 12 Nodes capable for classic CAN and CAN-FD are available through these headers.

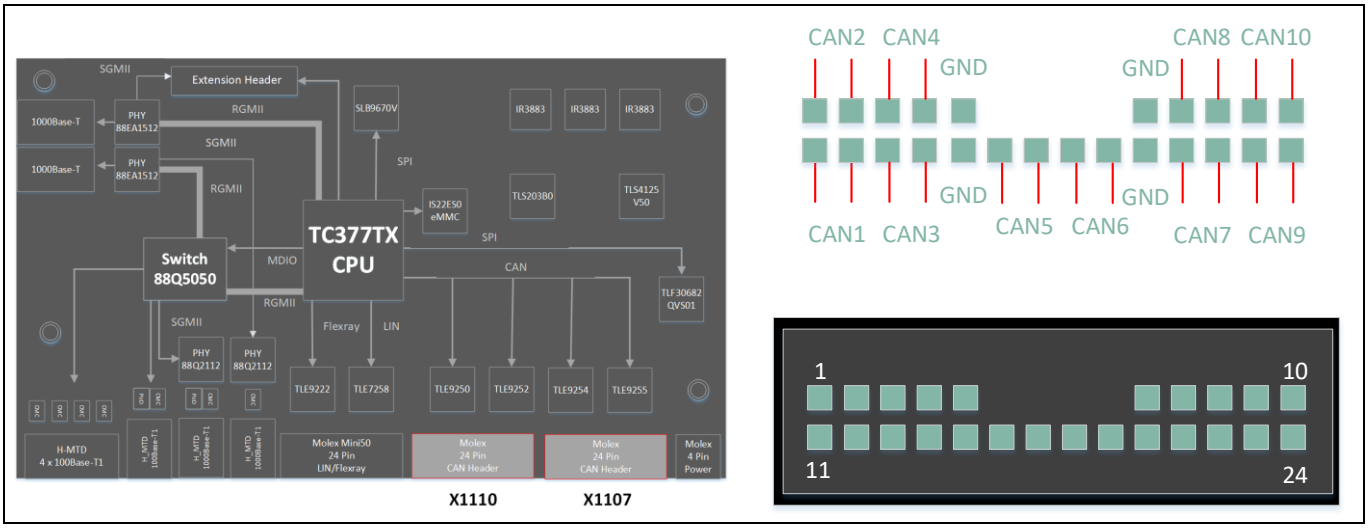

Figure 15 Molex Mini50 CAN-FD signal coding

2.9.1 CAN-FD Signals on Molex connectors

In sum the Secure Gateway-V1.1provides 12 CAN-FD channel with different Infineon CAN transceivers like the TLE9250, TLE9252, TLE9254, TLE9255 allowing exercising partial Network capabilities. This connectors are colored gray on that board.

Table 8Table 10 shows the CAN-FD signal connection list of connector X1107.

Table 8 CAN-FD Signal List Header X1107

Module	Signal	Pin	Header	Comment
CAN1	CAN13_RXDB	P33.5	X1107.12 CAN_H	CAN 1 Node 3
CAN1	CAN13_TXD	P33.4	X1107.11 CAN_L	CAN 1 Node 3
CAN1	CAN_WAKE1	P33.6	N.C	
CAN1	EN[1]	P02.9	N.C	Enable CAN 1 Node 3
CAN1	NERR	P40.0	N.C	
CAN1	INH	P33.1	N.C	
CAN2	CAN22_RXDA	P33.13	X1107.2 CAN_H	CAN 2 Node 2
CAN2	CAN22_TXD	P33.12	X1107.1 CAN_L	CAN 2 Node 2
CAN2	CAN_WAKE2	P33.7	N.C	
CAN2	EN[2]	P02.10	N.C	Enable CAN 2 Node 2
CAN2	NERR	P40.1	N.C	
CAN2	INH	P33.2	N.C	
CAN2	CAN20_RXDC	P34.2	X1107.17 CAN_H	CAN 2 Node 0
CAN2	CAN20_TXD	P34.1	X1107.16 CAN_L	CAN 2 Node 0
CAN2	CAN_WAKE3	P33.8	N.C	
CAN2	INH	P33.3	N.C	
CAN0	CAN03_RXDA	P00.3	X1107.4 CAN_H	CAN 0 Node 3
CAN0	CAN03_TXD	P00.2	X1107.3 CAN_L	CAN 0 Node 3
CAN0	WAKE	P32.1	N.C	
CAN0	INH	P32.0	N.C	
CAN1	CAN10_RXDA	P00.1	X1107.9 CAN_H	CAN 1 Node 0
CAN1	CAN10_TXD	P00.0	X1107.10 CAN_L	CAN 1 Node 0
CAN1	CAN11_RXDA	P00.5	X1107.19 CAN_H	CAN 1 Node 1
CAN1	CAN11_TXD	P00.4	X1107.18 CAN_L	CAN 1 Node 1

[1] Enable signal must be handled in customer software for proper operation of the CAN transceiver

[2] Enable signal must be handled in customer software for proper operation of the CAN transceiver

CAN1	CAN12_RXDB	P10.8	X1107.22 CAN_H	CAN 1 Node 2
CAN1	CAN12_TXD	P10.7	X1107.21 CAN_L	CAN 1 Node 2
CAN2	CAN23_RXDA	P14.9	X1107.7 CAN_H	CAN 0 Node 3/ CAN 2 Node 1
CAN2	CAN23_TXD	P14.10	X1107.8 CAN_L	CAN 0 Node 3/ CAN 2 Node 1
CAN12/23/10/11	STB1/STB2	P01.7	N.C	Standby Module

Table 10 shows the CAN-FD signal connection list of connector X1107.

Table 9 CAN-FD Signal List Header X1110

Module	Signal	Pin	Header	Comment
CAN2	CAN21_TXD	P20.3	X1110.10 CAN_H	CAN 2 Node 1
CAN2	CAN21_RDXC	P32.2	X1110.9 CAN_L	CAN 2 Node 1
CAN2	CAN21_STB/CAN00_STB	P33.0	N.C	Standby CAN21/00
CAN0	CAN00_RXDA	P02.1	X1110.8 CAN_H	CAN 0 Node 0
CAN0	CAN00_TXD	P02.0	X1110.7 CAN_L	CAN 0 Node 0
CAN0	CAN01_RXDC	P01_4	X1110.4 CAN_H	CAN 0 Node 1
CAN0	CAN01_TXD	P01_3	X1110.3 CAN_L	CAN 0 Node 1
CAN0	CAN02_RXDB	P02.3	X1110.2 CAN_H	CAN 0 Node 2
CAN0	CAN02_TXD	P02.2	X1110.1 CAN_L	CAN 0 Node 2

2.10 Molex Mini50 FlexRay™ LIN PSI5S

The Molex Mini 50 connector X1105 combines Flexray, LIN and general purpose signal connections. This connector is colored black on that board. Figure 16 show the connection scheme of that connector.

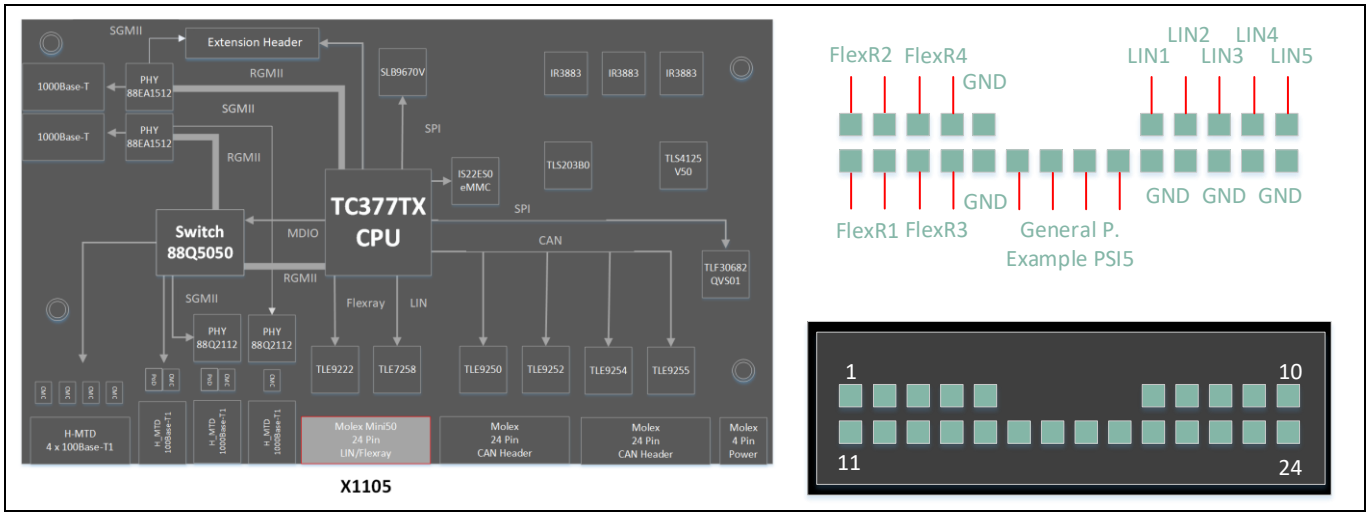

Figure 16 Molex Mini50 FlexRay™ LIN signal coding

2.10.1 FlexRay™

There are 2 FlexRay™ channel available on the Secure Gateway-V1.1 with Infineon's TLE9222 transceiver. In addition to the standard FlexRay™ signals, several control signals are added on PCB between AURIX and the FlexRay™ transceivers.

Table 10 shows the FlexRay™ signal connection list.

Table 10 FlexRay™ Signal List

Module	Signal	Pin	Header X1105	Comment
ERAY0	RXDA	P14.1	FR1_P – pin 9	ERAY-A_A - ERAY0_RXDA3 – U701
ERAY0	TXD	P14.0	FR1_N – pin 10	ERAY-A_A - ERAY0_TXDA – U701
ERAY0	TXDEN	P02.4	N.C	ERAY0_TXENA
I/O	STBN	P13.0	N.C	Zero Ohm R262 resistor (assembled)
I/O	ERRN	P40.2	N.C	
I/O	BGE	P13.3	N.C	
ERAY0	RXD	P14.7	FR2_P – pin 7	ERAY-B_A - ERAY0_RXDB0 – U703
ERAY0	TXD	P14.5	FR2_N – pin 8	ERAY-B_A - ERAY0_TXDB – U703
ERAY0	TXDEN	P14.6	N.C	ERAY0_TXENB
I/O	STBN	P15.7	N.C	Zero Ohm R263 resistor (assembled)
I/O	ERRN	P40.3	N.C	
I/O	BGE	P15.8	N.C	

2.10.2 LIN

There are 2 LIN channels available on the Molex connector X1105 of the Secure Gateway-V1.1 using Infineon's TLE7258.

Table 11 shows the LIN signal connection list.

Table 11 LIN Signal List

Module	Signal	Pin	Header X1105	Comment
ASCLIN2	RXD	P14.3	Pin 2	ASCLIN2_ARXA
ASCLIN0	TXD	P14.2	N.C	ASCLIN2_ATX
I/O	EN	P20.1	N.C	Zero Ohm R264 resistor (assembled)
ASCLIN6	RXD	P32.6	Pin 1	ASCLIN6_ARXC
ASCLIN6	TXD	P32.7	N.C	ASCLIN6_ATX
I/O	EN	P20.9	N.C	Zero Ohm R265 resistor (assembled)

2.11 QSPI channels

There are 4 QSPI channels available on the Secure Gateway-V1.1. Using various chip select lines allow addressing for several slave ICs like the PMIC device TLF30682QVS01, as well as CAN and Flexray transceivers.

Table 12 shows the QSPI signal connection list.

Table 12 QSPI connection list

Module	Signal	Pin	Device connected	Comment
QSPI3	MRSTA	P02.5		Master receive slave transmit
QSPI3	MTSR	P02.6		Master transmit slave receive
QSPI3	SCLK	P02.7		Clock output
QSPI3	SLSO5	P02.8	U604 TLE9255WLC	Slave select output 5
QSPI3	SLSO6	P00.8	U701 TLE9222PX	Slave select output 6
QSPI3	SLSO7	P00.9	U605 TLE9255WLC	Select slave output 7
QSPI3	SLSO8	P10.5	U703 TLE9222PX	Slave select output 8
QSPI1	MRSTA	P10.1		Master receive slave transmit
QSPI1	MTSR	P10.3		Master transmit slave receive
QSPI1	SCLK	P10.2		Clock output
QSPI1	SLSO10	P10.0	Extension Header	Slave select output 10
QSPI2	MRSTA	P15.4		Master receive slave transmit
QSPI2	MTSR	P15.5		Master transmit slave receive
QSPI2	SCLK	P15.6		Clock output
QSPI2	SLSO0	P15.2	U301 SLB9670VQ2.0	Slave select output 0
QSPI4	MRST	P22.1		Master receive slave transmit
QSPI4	MTSR	P22.0		Master transmit slave receive
QSPI4	SCLK	P22.3		Clock output
QSPI4	SLSO3	P22.2	U101 TLF30682QVS01	Slave select output 3

2.12 eMMC NAND flash memory

For Data storage like for example Firmware images an eMMC NAND flash memory of 4GB is on the Secure Gateway-V1.1This eMMC is connected to AURIX™ SDMMC module. Typically eMMC devices from ISSI are used. Storage size of the eMMC may differ between boards, please always check the device mounted on the Board.

Table 13 eMMC connections

Module	Signal	Pin	Comment
SDMMC	DAT0	P20.07	
SDMMC	DAT1	P20.08	
SDMMC	DAT2	P20.10	
SDMMC	DAT3	P20.11	
SDMMC	DAT4	P20.12	
SDMMC	DAT5	P20.13	
SDMMC	DAT6	P20.14	
SDMMC	DAT7	P15.00	
SDMMC	CLK	P15.01	
SDMMC	CMD	P15.03	
GPIO	/RST	P00.06	

To find out more about ISSI eMMC product please contact the listed contact partner in Appendix A.

2.13 General Purpose LEDs

The Secure Gateway-V1.1supports one own RGB LED and 2 general purpose LED connected to the pins listed Table 14.

Table 14 LEDs TC377TX

Module	Signal	Pin	Comment
GPIO	BLUE	P33.14	
GPIO	BLUE	P34.4	
GPIO	GREEN	P33.15	RGB Led
GPIO	RED	P34.5	RGB Led
GPIO	BLUE	P34.3	RGB Led

2.14 Extension Header X1109

Next to the two RJ45 Connectors a signal extension Header is available for extending use case of the Secure Gateway-V1.1. Beside the HSSL interface, a QSPI with two chip select signals and one I2C channel a SGMII 1Gb/s interface is available.

Table 15 Extension Header CPU

Module	Signal	Pin	Pin on Header	Comment
QSPI1	MRSTA	P10.1	4	Master receive slave transmit
QSPI1	MTSR	P10.3	8	Master transmit slave receive
QSPI1	SCLK	P10.2	6	Clock output
QSPI1	SLSO8	P10.4	10	Slave select output 8
QSPI1	SLSO10	P10.0	2	Slave select output 10
I2C	SCL	P13.1	20	
I2C	SDA	P13.2	22	
HSSL	SYSCLK		13	
HSSL	HSCT0_RXD_P		15	
HSSL	HSCT0_RXD_N		17	
HSSL	HSCT0_TXD_P		19	
HSSL	HSCT0_TXD_N		21	
88EA1512	SGMII TX N		1	U1001
88EA1512	SGMII TX P		3	U1001
88EA1512	SGMII RX N		5	U1001
88EA1512	SGMII RX P		7	U1001
GND			9, 11, 14, 16, 18	
+3,3V			12	

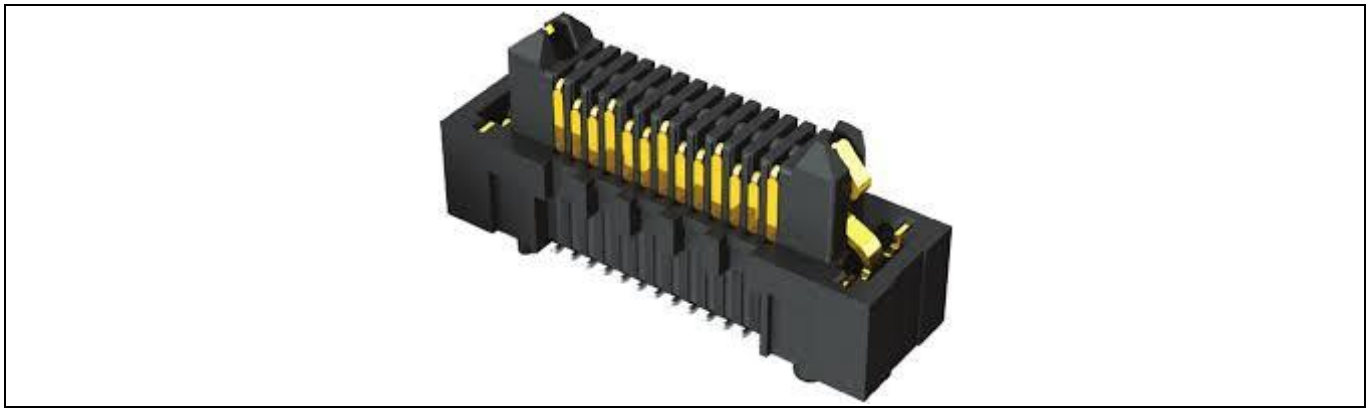

Figure 17 Samtec ASP-137968-01

3 Software initialization sequence

For example projects please refer to Infineon MyCIP system. There you will find software examples for the AURIX™ TC377TX.

Marvell Ethernet components shell boot up automatic by its own. In the AURIX™ only basic support for these components is given in form of binary libraries. Please contact Marvell for requesting the API Software examples for the PHY and Switch.

Depending on Board soldering options the GPIO P21.1 must be taken care. This pin can reset the complete Marvell components and per default be pulled low. This would lead to a permanent reset, signalized with the red LED (D201).

The device U901 (88Q2112) is per default set to reset. The device is connected via SGMII to U1000 (88EA1512) which can bridge the port 6 of the 88Q5050 between copper interface and SGMII. To use port 6 as 1000Base-T1 port the AURIX pin P32.3 must be set to high.

4 Schematic and PCB

The schematic and layout data can be requested by Infineon as long the user has a valid NDA with Marvell. Please contact either Infineon or Marvell contacts for that.

5 Appendix A

For future information about the Infineon products, Marvell IC's, ISSI eMMC and Rosenberger connectors please contact the companies below.

Infineon Technologies AG	Marvell	Rosenberger
Infineon Technologies AG Am CAMPEON 1-12 85579 Neubiberg, Germany Contact: **http://www.infineon.com/productsupport** www.infineon.com	Marvell Semiconductor, Inc. - Santa Clara United States Headquarters 5488 Marvell Lane Santa Clara, CA 95054 Mail : info@marvell.com https://www.marvell.com/company.html	Rosenberger Hochfrequenztechnik GmbH & Co. KG Hauptstraße 1 83413 Fridolfing P.O. Box 1260 84526 Tittmoning Germany Phone +49 8684 18-0 info@rosenberger.com www.rosenberger.com

ISSI		
Integrated Silicon Solution Inc 1623 Buckeye Drive Milpitas, CA 95035 **http://www.issi.com**		

Molex Connector information

Power Supply	CAN	LIN / Flexray
Molex Part Number: 347910040  Mini50 Unsealed Receptacle, Single Row, Non-Bridged, 4 Circuits, Polarization Option A, Black	**Molex** Part Number: 348240245  Mini50 Unsealed Receptacle, Dual Row, Non-Bridged, 24 Circuits, EcoPaXX Resin, Polarization Option B, Gray	**Molex** Part Number: 348240244  Mini50 Unsealed Receptacle, Dual Row, Non-Bridged, 24 Circuits, EcoPaXX Resin, Polarization Option A, Black

Revision history

Major changes from V1.0 to V1.1 of the manual

Page or reference	Description of change
11	Correct Table for Ethernet MAC connections in chapter
9	Add Current measurement channel into the table

Major changes from V1.1 to V1.2 of the manual

Page or reference	Description of change
4	Change block diagram for being compatible with design (swap port P6 and P7)
14	Correct Table for PoDL handling
5	Change picture to Board version V1.1

Edition 2020-11-16

Published by

Infineon Technologies AG

81726 Munich, Germany

Do you have a question about this document?

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Document reference
Board Manual